IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.:	10/659,320
Applicants:	Munter et al.
Filing Date:	September 11, 2003
Art Unit:	2616
Examiner:	Tsegaye, Saba
Confirmation No.:	3794
Title:	High Throughput Rotator Switch Having Excess Tandem Buffers

Commissioner for Patents
Mail Stop Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

In response to the Office Action, dated June 27, 2008, rejecting pending claims 1-25, and in support of the Notice of Appeal received by the U.S. Patent and Trademark Office on September 26, 2008, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences. Authorization is herein granted to apply the $510.00 requisite fee set forth in 37 C.F.R. §41.20(b)(2), and any other fees or credits due in this case to Deposit Account No. 122158. Appellants respectfully request reconsideration and reversal of the Examiner's rejections of the pending claims.

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The Real Party in Interest is Nortel Networks Ltd., the owner of all rights of this patent application by virtue of an assignment recorded at reel and frame number 014477/0001.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

The patent application as originally filed included claims 1 - 25. Claims 1 and 24 were amended in an Amendment and Response dated September 27, 2007 in response to a non-final Office Action mailed May 31, 2007. Claims 1, 13, 17, and 25 were amended in an Amendment and Response dated March 28, 2008 in response to a non-final Office Action mailed December 28, 2007. A final Office Action mailed June 27, 2008 rejects claims 1 - 25. Accordingly, claims 1 - 25 are pending in the application and are the subject of this appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final Office Action.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1

Appellants' invention, as recited in independent claim 1, features a communications switch for switching data between inputs and outputs. Claim 1 is summarized with reference to Fig. 2 and paragraphs [0027] – [0029] of the Appellants' specification. The communications switch 30 (Fig. 2) includes p inputs (input buffers 32, Fig. 2 [0027]) each for receiving data to be switched to q outputs (output buffers 44, Fig. 2 [0028]). The communications switch 30 also includes p+k information storage buffers 38 (tandem buffers 38, Fig. 2 [0027]). Each of the information storage buffers includes p+k storage locations. The communications switch 30 further includes an input data conditioner (data conditioner 34, Fig.2 [0028]), having p inputs and p+k outputs, connected between said p inputs of the communications switch 30 and the p+k information buffers 38. The input data conditioner 34 is for distributing data received at the p inputs of the input data conditioner 34 to its p+k outputs. The communications switch 30 further includes an ingress commutator (36, Fig. 2 [0027]) for interconnecting each of the p+k information storage buffers 38 to one of the p+k outputs of the input data conditioner 34, and an output data conditioner (data conditioner 42, Fig. 2 [0028]) having p+k inputs and q outputs, for distributing data from its p+k inputs to its q outputs. The switch 30 further includes an egress commutator (40, Fig.2 [0027]) for interconnecting each of said p+k information storage buffers (tandem buffers 38) to one of the p+k inputs of said output conditioner (data conditioner 42, Fig. 2 [0028]). The ingress commutator 36 is operable to cyclically interconnect each of the p+k outputs of the input data conditioner 34 to each of the p+k information buffers 38 to provide data from the p+k outputs of the input data conditioner 34 to the p+k information storage buffers 38. The egress commutator 40 is operable to cyclically interconnect each of the p+k information storage buffers (38 to the p+k inputs of the output data conditioner 42 to provide data from the p inputs 32 to the q outputs 44, wherein p, q, and k are positive integers.

Independent claim 13

Appellants' invention, as recited in independent claim 13 features a communications switch. Claim 13 is summarized with reference to Fig. 2 and paragraphs [0027] – [0029] of the Appellants' specification. The communications switch 30 (Fig. 2) has p inputs 32 (input buffers 32, Fig. 2 [0027]) and q outputs 44 (output buffers 44, Fig. 2 [0028]). The switch 30 further has a rotator switch 46 having a (p+k)x(p+k) switch fabric (Fig 2, switch fabric 46, [0028], (p+k)x(p+k) tandem buffers 38)). The switch 30 also includes an input data conditioner 34 (Fig. 2, 34, [0028]) for distributing data received at the p inputs 32 to the switch fabric 30, and an output data conditioner 42 (Fig. 2, 42, [0028]) in communication with the switch fabric 46 for distributing data received from the switch fabric to said q outputs 44, wherein p, q, and k are positive integers.

Independent claim 17

Appellants' invention, as recited in independent claim 17 features a method of switching data between p inputs and q outputs. The method includes the step of distributing data from said p inputs to p+k intermediate inputs (Fig. 2, [0030], "traffic to be switched through switch 30 arrives at the input buffers 32", [0031], "the input data condition receives p+k entities of input data at each if its inputs", … the input data conditioner distributes the p input data entities and their associated overheads to the p+k output, providing an intermediate input to switch fabric 46"). The method also includes the step of loading data from said p+k inputs into p+k tandem buffers, each of said tandem buffers comprising p+k storage locations (Fig. 2, [0032] "ingress commutator 36 cyclically interconnects the p+k outputs of data conditioner 34 to p+k tandem buffers 38"). The method further includes the step of unloading one location of each of said p+k tandem buffers at one of p+k intermediate outputs (Fig. 2, [0033]), and the step of combining data from said p+k intermediate outputs to provide switched data from said p inputs at said q outputs, wherein p, q, and k are positive integers (Fig. 2, [0033], egress commutator 40 similarly interconnects the tandem buffers 38 to the p+k inputs of output data conditioner 42. … output data conditioner 42 combines data from the p+k tandem buffers 38 to form q outputs, provided at its outputs to output buffers 44.)

Independent claim 25

Appellants' invention, as recited in independent claim 25 features a communications switch for switching information units between inputs and outputs. Claim 25 is summarized with reference to Fig. 2 and paragraphs [0027] – [0029] of the Appellants' specification. The communications switch 30 (Fig. 2) includes p inputs (input buffers 32, Fig. 2 [0027]) each for receiving data to be switched to q outputs (output buffers 44, Fig. 2 [0028]). The switch 30 also includes p+k information storage buffers 38 (tandem buffers 38, Fig. 2 [0027]), each of the information storage buffers 38 having p+k storage locations. The switch 30 includes means for distributing data received at the p inputs to p+k intermediate inputs. This means for distributing can be realized for example as an input data conditioner (data conditioner 34, Fig.2 [0028]). The switch 30 further includes means for cyclically interconnecting each of the p+k intermediate inputs to one of the p+k information storage buffers. This means for cyclically interconnecting can be realized for example as an ingress commutator (36, Fig. 2 [0027]). The switch 30 further includes means for distributing data from said p+k information storage buffers to said p outputs. This means for distributing can be realized for example as an output data conditioner (data conditioner 42, Fig. 2 [0028]). The switch 30 also includes means for cyclically interconnecting each of said p+k information storage buffers to said means for distributing data from said p+k information storage buffers. This means for cyclically interconnecting can be realized for example as an egress commutator (40, Fig.2 [0027]). Again, p, q, and k are positive integers.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Office Action issued the following rejection:

I. Claims 1-25 are rejected under 35 U.S.C. § 102 (e) as being anticipated by Fisher et al. (U.S. Patent Publication 2002/0039362 A1).

Accordingly, the grounds of rejection to be reviewed on appeal are grounds I as applied to claims 1-25.

ARGUMENT

Rejection under 35 U.S.C. § 102(e) as being anticipated by Fisher et al. (U.S. Patent Publication 2002/0039362 A1).

The final Office Action rejects claims 1-25 as being anticipated by Fisher et al. (U.S. Patent Publication 2002/0039362 A1) (hereinafter "Fisher").

A prima facie case of anticipation requires a showing of each and every element of the claim within the four corners of the cited reference. The Appellants assert that Fisher fails to teach or suggest each and every element of the Claims.

Claims 1 and 25

In rejecting claims 1 and 25, the Office Action refers to Fig. 6 of Fisher. Particularly, the Office Action refers to s0-s3 as representing inputs (presumably Fisher Fig. 6 Source 0 – Source 3), d0-d3 as representing outputs (presumably Fisher Fig. 6 Dest. 0 – Dest. 3), and t(0,0) –t(3,1) as representing "p+k information storage buffers, each of said information storage buffers comprising p+k storage locations (t(0,0-t(3,1)). The Office Action then refers to "an input data conditioner (152, 154, 162, 164) comprising p inputs and p+k outputs, connected between said p inputs of said communications switch and said p+k information buffers (t(0,0)-t(3,1)), for distributing data received at said p (s0-s3) inputs of said input data conditioner to its p+k outputs", "an ingress commutator (90, 92, 94, 96) for interconnecting each of said p+k information storage buffers to one of said p+k outputs of said input data conditioner (see fig. 6; 0049); an output data conditioner (156, 158, 166, 168) comprising p + k inputs a q (d0 – d3) outputs, for distributing data from its p+k inputs to its q (d0-d3 outputs (see fig. 6; 0049-0051); an egress commutator (120, 122, 124, 126) for interconnecting each of said p+k information storage buffers (t(0,0)-t(3,1)) to one of said p+k inputs of said output

conditioner (156, 158, 166, 168); said ingress commutator (90,92, 94, 96) operable to cyclically interconnect each of said p+k outputs of said input data conditioner (152, 154, 162, 164) to each of said p+k information buffers (t(0,0 –t(3,1) to provide data from said each of said p+k outputs of said input data conditioner (152, 154, 162, 164) to said p+k information storage buffers (t(0,0)-t(3,1)), said egress commutator (120, 122, 124, 126) operable to cyclically interconnect each of said p+k information storage buffers (t(00)-t(3,1)) to said p+k inputs of q (d0-d3) outputs (see fig. 6; 0049 – 0051).

The Appellants respectfully disagree with the characterizations of Fisher as set forth in the Office Action.

Fig. 6 of Fisher is a specific implementation of an embodiment of Fig. 5 of Fisher (Fisher [0047]) – thus Fig. 5 can simplify the understanding of Fig. 6. In Fig. 5 of Fisher, there is shown a rotator switch wherein source bandwidth is divided across several "rotators" in different planes (Fisher [0041]). Thus, each source node is able to connect to alternate pairs of switches – i.e. source 0 is now able to send either an IU to each of two rotators at half the rate, or half an IU to one rotator plane and the second half to the second rotator plane (Fisher [0043]). The method of Fig. 5 involves dividing one rotator into a multiplicity of smaller rotators (Fisher [0043]).

In Fig. 6, the source nodes are separated from the switches by multiplexers. That is, the sources are separated into modules 140 and 142. Source node module 140 includes sources s0-s3, while source node module 142 includes sources s4-s7. Switching module 150 includes the first plane 130 of Fig. 5, while switching module 160 includes the second plane 132. The source node modules 140 and 142 are coupled to the switching modules 150 and 160 via multiplexers 144, 145, 146, 148, 152, 154, 162, and 164. The difference between Fig. 6 and Fig. 5 of Fisher is that the source (and destination) nodes have modularized and multiplexed/demultiplexed from the core of the rotator (Fisher [0051]).

In accordance with the Applicants' invention, and in contrast with Fisher, a communications switch has p inputs to be switched to q outputs, and has p+k information storage buffers. An input data conditioner comprises p inputs and p+k outputs, connected between said

p inputs of said communications switch and said p+k information buffers, for distributing data received at said p inputs of said input data conditioner to its p+k outputs. Note, then, that p inputs are coupled via the input data conditioner to a p+k rotator. This is different than a system wherein the rotator is divided into a multiplicity of smaller rotators.

The Office Action, in its rejection of Claims 1 and 25, takes Fig. 6 of Fisher in piece-part. The Office Action suggests that the (s0-s3) inputs represent the claimed "p inputs", and the (d0-d3) outputs represent the claimed "q outputs", even though Fig. 6 of Fisher shows 8 inputs (s0 – s7) and 8 outputs (d0 – d7). The Office Action then asserts that Fisher discloses "an input data conditioner (152, 154, 162, 164) comprising p inputs and p+k outputs, connected between said p inputs of said communications switch and said p+k information buffers (t(0,0)-t(3,1)), for distributing data received at said p (s0-s3) inputs of said input data conditioner to its p+k outputs", thus suggesting that the input data conditioners of Appellants' invention are shown by the four (s0-s3) inputs and eight multiplexer outputs of Fisher, when in fact the multiplexers are fed by inputs (s0 – s7).

The Appellants disagree with this assertion because, if in fact Fig. 6 of Fisher only showed inputs (s0-s3) and outputs (d0-d3), then, as taught in Fig. 5 of Fisher, there would only be four tandem buffers and switches shown – or two – or one – and therefore fewer multiplexers. For this reason, the Appellants maintain that Fisher fails to teach or suggest, and therefore cannot anticipate, the Appellants' claimed invention including "an input data conditioner, comprising p inputs and p+k outputs, connected between said p inputs of said communications switch and said p+k information buffers, for distributing data received at said p inputs of said input data conditioner to its p+k outputs" as set forth in Claim 1. The Appellants likewise maintain that Fisher fails to anticipate the Appellants' claimed invention as set forth in Claim 25 including "means for distributing data received at said p inputs to p+k intermediate inputs".

The Final Office Action offered a response to Applicant's Arguments filed on March 28, 2008. The Office Action states, "Fisher discloses a rotator switch having a multiplexing group of K1 sources onto one tandem rotator switch comprising: a first commutator connected to the multiplexed outputs; a plurality of intermediate nodes connected to the first commutator; and a second commutator connected to the intermediate nodes and having a plurality of multiplexed outputs. As shown in fig. 6, the first commutator (input data

conditioner) comprising multiplexed inputs (p inputs) and p+k outputs, connected between the P inputs and the plurality of intermediate nodes (buffers). The second commutator (output data conditioner) connected to the plurality of intermediate nodes (buffers) having a plurality inputs (p+k) and multiplexed outputs (q outputs).

The Appellants disagree with this reasoning as well. If the commutators (i.e. Fig. 1 26, [0025], Fig. 6 90, 92, 94, 96, unidentified in Office Action) are considered the input data conditioner, then they have they have the same numbers of inputs and outputs- i.e. there is no data conditioner having p inputs and p+k outputs. Thus, again, Fisher fails at least to anticipate the Applicants' claimed invention as set forth in Claims 1 and 25.

Claim 13

Regarding Claim 13, the Office Action asserts that Fisher discloses "a communications switch (see Fig. 6), comprising p inputs (s0-s3) and q outputs (d0-d3); a rotator switch comprising a (p+k)x(p+k) switch fabric (150, 160); and input data conditioner (152, 154, 162, 164) for distributing data received at the p inputs to that switch fabric (0048);…"

Appellants assert that Fisher fails to anticipate a communications switch comprising "a rotator switch comprising a (p+k)x(p+k) switch fabric" and "an input data conditioner for distributing data received at said p inputs to said switch fabric" for the same reasons as set forth with regard to Claim 1 above.

Claim 17

Regarding Claim 17, the Office Action asserts that Fisher discloses a method of switching data between p (s0-s3) inputs and q outputs (d0-d3), comprising: distributing data from said p inputs to p+k intermediate inputs (demultiplexer 152, 154, 162, 164 connected to each commutator 90, 92, 94, 96)… Appellants assert that Fisher fails to anticipate Claim 17 for the same reasons as set forth above with regard to Claim 1.

Claims 2 – 12, 14 – 16, and 18 – 24

Regarding Claims 2 – 12, 14 – 16, and 18 – 24, each of these dependent claims depends from allowable claim 1, 13, 17, or 25 and incorporates all of its limitations. Therefore, Appellants submit that dependent claims 2 – 12, 14 – 16, and 18 – 24 are allowable at least for the reasons provided above with respect to the independent claims.

CONCLUSION

In view of the arguments made herein, Appellants submit that the application is in condition for allowance.

Respectfully submitted,

Date: November 26, 2008
Reg. No. 37,946

/Mary Steubing/
Mary Steubing
Attorney for Appellants
Guerin & Rodriguez, LLP
5 Mount Royal Avenue
Marlborough, MA 01752

Tel. No.: (508) 303-2003
Fax No.: (508) 303-0005

CLAIMS APPENDIX

1. A communications switch for switching data between inputs and outputs, said communications switch comprising:

p inputs each for receiving data to be switched to q outputs;

p+k information storage buffers each of said information storage buffers comprising p+k storage locations;

an input data conditioner, comprising p inputs and p+k outputs, connected between said p inputs of said communications switch and said p+k information buffers, for distributing data received at said p inputs of said input data conditioner to its p+k outputs;

an ingress commutator for interconnecting each of said p+k information storage buffers to one of said p+k outputs of said input data conditioner;

an output data conditioner comprising p+k inputs and q outputs, for distributing data from its p+k inputs to its q outputs;

an egress commutator for interconnecting each of said p+k information storage buffers to one of said p+k inputs of said output conditioner;

said ingress commutator operable to cyclically interconnect each of said p+k outputs of said input data conditioner to each of said p+k information buffers to provide data from said each of said p+k outputs of said input data conditioner to said p+k information storage buffers, said egress commutator operable to cyclically interconnect each of said p+k information storage buffers to said p+k inputs of said output data conditioner to provide data from said p inputs to said q outputs;

wherein p, q, and k are positive integers.

2. The switch of claim 1, where p=q.

3. The switch of claim 1, wherein said ingress commutator is clocked at a rate to transfer less data to each of said p+k information storage buffers during a time interval than is received at each of said p inputs during said time interval.

4. The switch of claim 1, wherein said ingress commutator is clocked at a rate of 1/t to transfer data to each of said information buffers arriving at said input at a rate of 1/t' where t' = t*p/(p+k).

5. The switch of claim 1, wherein said input data conditioner comprises 2p(p+k) buffers for storing data received at said p inputs of said data conditioner.

6. The switch of claim 5, wherein said input data conditioner comprises p, (1 input, 2(p+k) output) data distributors each to present data at one of said inputs of said input data conditioner to one of said buffers.

7. The switch of claim 6, wherein said input data conditioner comprises p, 2(p+k) input data selectors, each to select data from one of said buffers to one of p of said p+k outputs of said input data conditioner.

8. The switch of claim 7, wherein said input data conditioner comprises k, p input, one output data selectors, for selecting from one of its p inputs data to be output at one of k of said p+k outputs of said input data conditioner.

9. The switch of claim 1, wherein said output data conditioner comprises k one input, p output switches, each for switching data from its input to one of its p outputs.

10. The switch of claim 9, wherein said output data formatting block comprises p k+1 input, 2(p+k) output switches for ordering data units received at said p+k inputs of said output data formatting block.

11. The switch of claim 10, wherein said output data formatting block comprises p sets of 2(p+k) intermediate buffers, each in communication with one of said p output switches.

12. The switch of claim 11, wherein said output data formatting block comprises p 2(p+k) input, one output data distributors, each for providing an output from said data conditioner from one set of said intermediate buffers.

13. A communications switch, comprising:

p inputs and q outputs;

a rotator switch comprising a (p+k)x(p+k) switch fabric;

an input data conditioner for distributing data received at said p inputs to said switch fabric;

an output data conditioner in communication with said switch fabric for distributing data received from said switch fabric to said q outputs;

wherein p, q, and k are positive integers.

14. The communication switch of claim 13, wherein p=q.

15. The communications switch of claim 14, wherein said rotator switch comprises p+k information storage buffers and wherein said switch fabric is clocked at a rate so as to switch less traffic through each of said p+k information buffers than arrives at one of said inputs in a clock cycle.

16. The communications switch of claim 15, wherein said rotator switch comprises p+k information storage buffers and wherein said switch fabric is clocked at a rate so as to transfer an amount of traffic through said p+k information buffers equaling at least an amount arriving at all of said p inputs in said clock cycle.

17. A method of switching data between p inputs and q outputs, comprising:

distributing data from said p inputs to p+k intermediate inputs;

loading data from said p+k inputs into p+k tandem buffers, each of said tandem buffers comprising p+k storage locations;

unloading one location of each of said p+k tandem buffers at one of p+k intermediate outputs;

combining data from said p+k intermediate outputs to provide switched data from said p inputs at said q outputs;

wherein p, q, and k are positive integers.

18. The method of claim 17, further comprising cyclically interconnecting said p+k tandem buffers with said p+k intermediate inputs and said p+k intermediate outputs.

19. The method of claim 18, wherein data is loaded into said tandem buffers at a rate lower than a rate of traffic arriving at each of said p inputs.

20. The method of claim 17 wherein data is loaded into all of said tandem buffers at a rate at least equal to a rate of arrival of data at all of said p inputs.

21. The method of claim 18, wherein said p+k tandem buffers are cyclically interconnected at a rate of 1/t to load data to each of said tandem buffers for data arriving at each of said inputs at a rate of 1/t', where t' = t*p/(p+k).

22. The method of claim 19, wherein at least some of said data is transferred to a selected location of an interconnected tandem buffer, said location based on a destination for said at least some of said data.

23. The method of claim 19, further comprising combining data into data units, and including a header in each of said data units, each header including destination information and a sequence number for said each of said data units.

24. The method of claim 23, wherein said combining further comprises stripping said headers from said data units.

25. A communications switch for switching information units between inputs and outputs, said switch comprising:

p inputs each for receiving data to be switched to q outputs;

p+k information storage buffers, each of said information storage buffers comprising p+k storage locations;

means for distributing data received at said p inputs to p+k intermediate inputs;

means for cyclically interconnecting each of said p+k intermediate inputs to one of said p+k information storage buffers;

means for distributing data from said p+k information storage buffers to said p outputs;

means for cyclically interconnecting each of said p+k information storage buffers to said means for distributing data from said p+k information storage buffers;

wherein p, q, and k are positive integers.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.